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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,180	10/29/2003	Masanori Minamio	10873.1334US01	8184

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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,180	MINAMIO ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *3 and 14-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10,12 and 13* is/are rejected.

7)☒ Claim(s) *7,9 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election **with traverse** of claims **1 – 2** and **4 – 13** in the reply filed on June 23, 2005 is acknowledged.

Because Applicant did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Claims **3** and **14 – 19** are withdrawn from further consideration as directed to a nonelected invention.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on October 29, 2003

Information Disclosure Statement

3. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on January 20, 2004.

Information disclosed and lists on PTO 1449 were considered.

Claim Objections

4. Claims **7** and **10** are objected to because of the following informalities:

Claim **7**, line 2: "the first semiconductor chip" should be changed to -- the semiconductor chip --;

Claim **10,** line 2: "ball electrodes" should be change to -- a plurality of ball electrodes --;

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims **1** and **2** are rejected under 35 U.S.C. 102(e) as being anticipated by Crowley et al. (US Patent No. 6,605,866).

Regarding claim **1**, Crowley discloses a lead frame 62 (figs. 2, 3 & 10), comprising:

a frame (figs. 3, 6 & 8) ; and

a plurality of inner leads 54, 75, 77, 83, 87 (figs. 2 – 14), extending inward from the frame, wherein the inner lead 54, 75, 77, 83, 87 includes a protruded portion provided on a surface of its outer portion, the protruded portion protrudes in a thickness direction, and a step portion is formed in a side portion of the protruded portion.

Regarding claim **2**, Crowley discloses the step portion is formed as a portion with two steps (figs. 4 – 14).

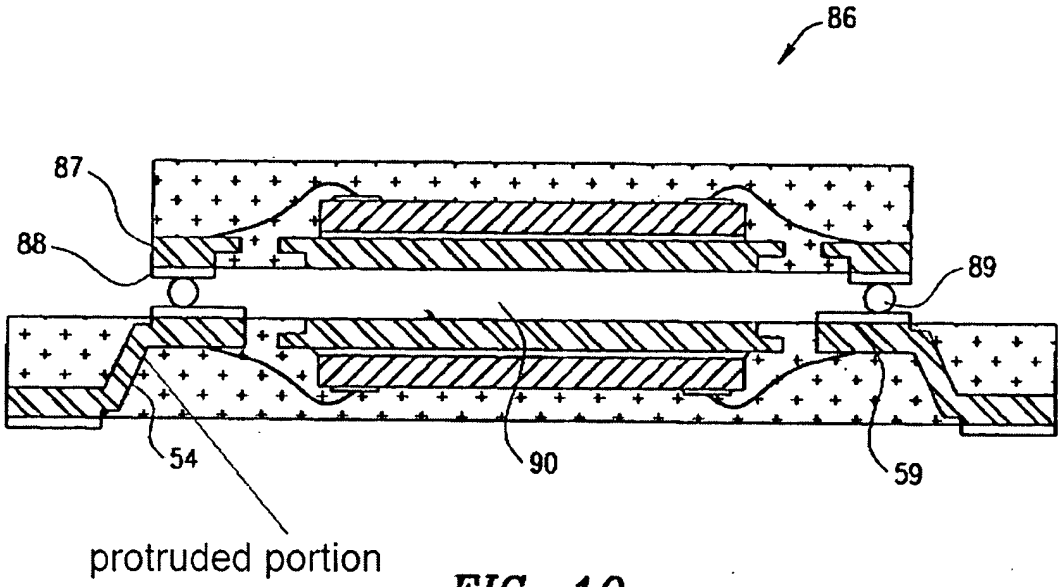


FIG. 10

7. Claims **4 – 8** are rejected under 35 U.S.C. 102(b) as being anticipated by Chun-Jen et al. (US Patent No. 6,337,510).

Regarding claim **4**, Chun-Jen discloses a resin-encapsulated semiconductor devices 100/200/300/400 (fig. 5), comprising:

a semiconductor chip 110/210/310/410 (figs. 1 – 6) having a group of electrodes (not labeled);

a plurality of inner leads 120/220/320/420 (figs. 1 – 6) that are arranged along a periphery of the semiconductor chip and are connected to the group of electrodes of the semiconductor chip, respectively; and

an encapsulating resin 140/240/340/440 (figs. 1 – 6; column 2, lines 61 – 62) that encapsulates a connection part located between the semiconductor chip and the inner leads 120/220/320/420, with a part of each of the inner leads being exposed from the

encapsulating resin to form an external terminal (upper surface and lower surface of the inner leads),

wherein the inner lead 120/220/320/420 includes a protruded portion provided on a surface thereof on an outer side relative to the periphery of the semiconductor chip 110/210/310/410, the protruded portion protruding in a thickness direction with a step portion formed in a side portion of the protruded portion,

the group of electrodes of the semiconductor chip is connected to surfaces of inner portions 122/322/422 (figs. 2,3,5 & 6; 422 not labeled; column 4, lines 18 – 19) of the inner leads 120/ 320/420 located on an inner side relative to their protruded portions, through electroconductive bumps 130/330/430 (figs. 1,3 5 & 6; column 4, lines 16 – 19), respectively, and

the encapsulating resin 140/340/440 encapsulates the semiconductor chip 110//310/410 and the electroconductive bumps 130/330/430 and is formed to expose surfaces of the protruded portions.

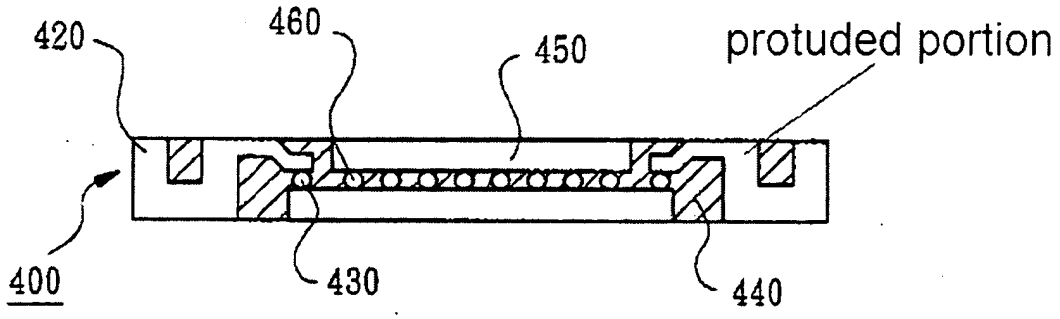


FIG. 6

Regarding claim **5**, Chun-Jen discloses a resin-encapsulated semiconductor device 400 (fig. 6) also includes a first semiconductor chip 410 (fig. 6; not labeled) and a second semiconductor chip 450 (fig. 6) that is stacked on a surface of the first semiconductor chip and has a smaller size than that of the first semiconductor chip 410 (column 4, lines 8 – 10),

the protruded portions of the plurality of inner leads 420 are located on an outer side relative to a periphery of the first semiconductor chip 410,

a first group of electrodes of the first semiconductor chip 410 (not label; column 4, lines 17 & 18) is connected with the surfaces of the inner portions 422 of the inner leads 420 located on the inner side relative to their protruded portions, through first electroconductive bumps 430 (fig. 6; column 4, lines 16 – 19), respectively,

the second semiconductor chip 450 is disposed within a region surrounded by inner ends of the plurality of inner leads 420 and is connected electrically with a second group of electrodes of the first semiconductor chip through second electroconductive bumps 460 (fig. 6; column 4, lines 12 – 16), and

the encapsulating resin 440 encapsulates surfaces of the first and second semiconductor chips 410, 450 and the first and second electroconductive bumps 430 and 460.

Regarding claim **6**, Chun-Jen discloses the surfaces of the protruded portions and an outer face of the encapsulating resin 440 are substantially in the same plane (fig. 6).

Regarding claim **7**, Chun-Jen discloses a back face of the first semiconductor chip 410 and an outer face of the encapsulating resin 440 are substantially in the same plane.

Regarding claim **8**, Chun-Jen discloses back faces of the inner leads 420 (fig. 6) and an outer face of the encapsulating resin 440 (fig. 6) are substantially in the same plane.

8. Claims **4, 10, 12** and **13** rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US Patent No. 6,303,997).

9. Regarding claim **4**, Lee discloses a resin-encapsulated semiconductor device 108/109/110 (figs. 11 – 13), comprising:

a semiconductor chip10 (figs. 11 – 13) having a group of electrodes 11 (figs. 11 – 13; column 6, lines 48+ and column 7, lines 38 – 44);

a plurality of inner leads 20 (figs. 11 – 13) that are arranged along a periphery of the semiconductor chip and are connected to the group of electrodes of the semiconductor chip, respectively; and

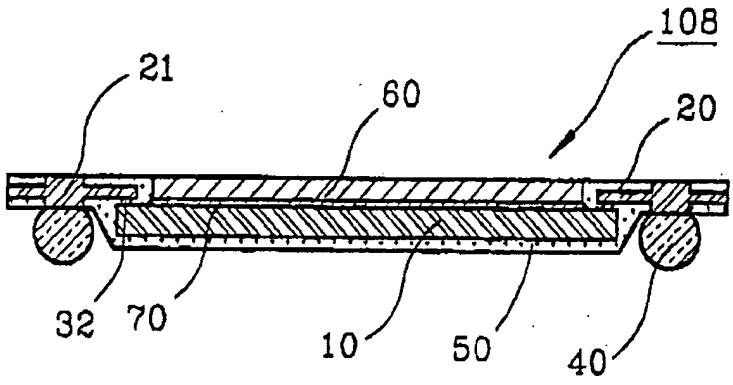
an encapsulating resin 50 (figs. 11 – 13) that encapsulates a connection part located between the semiconductor chip 10 and the inner leads 20, with a part of each of the inner leads 20 being exposed from the encapsulating resin 50 to form an external terminal (figs. 11 – 13; column 5, lines 31 – 38; column 6, lines 47 – 67; column 7, lines 1+; and column 8, lines 1 – 36)

wherein the inner lead 20 includes a protruded portion 21 (figs. 11 – 13) provided on a surface thereof on an outer side relative to the periphery of the semiconductor chip 10, the protruded portion 21 protruding in a thickness direction with a step portion formed in a side portion of the protruded portion 21,

the group of electrodes of the semiconductor chip is connected to surfaces of inner portions 20 (figs. 11 – 13) of the inner leads located on an inner side relative to their protruded portions, through electroconductive bumps 32 (figs. 11 – 13; column 7, lines 38 – 52), respectively, and

the encapsulating resin 50 encapsulates the semiconductor chip 10 and the electroconductive bumps 32 and is formed to expose surfaces of the protruded portions 21.

Fig. 11



Regarding claim **10**, Lee discloses ball electrodes 40 (fig. 11) are formed on the protruded portions 21.

Regarding claims **12** and **13**, Lee further teaches resin a plurality of encapsulated semiconductor devices, as disclosed in figs. 11 – 13, could be stacked on top of each other, and in adjacent pairs, back faces of inner leads of one are connected electrically with surfaces of protruded portions of an other as disclosed in fig. 3 (column 8, lines 24 – 30).

Allowable Subject Matter

10. Claims **9** and **11** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is an examiner's statement of reasons for the indication of allowable subject matter: Claims **9** and **11** are allowable over the prior art of record because none of the prior art ( ) whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

an inner lead 16 (fig. 1c) is tilted upward to a side on which a protruded portion protrudes and toward an inner end of the inner lead portion 16a as cited in claim 9; and an insulating thin film 33 (3A – 3C) formed on a part of a surface of a protruded portion 17 of each inner lead 16, the uncovered part of protruded portion 17 that not being covered by the insulating film 33 is used as an external terminal as cited in claim 11.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Paek (US Patent No. 6,700,187), Yang (US Patent No. 6,730,544) and Song (US Patent No. 5,471,088) disclose a semiconductor device similar to that of Crowley et al. (US Patent No. 6,605,866), of Chun-Jen et al. (US Patent No. 6,337510) and of Lee (US Patent No. 6,303,997).

13. A shortened statutory period for response to this action is set to expire e (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT

August 31, 2005